1	1	**All marks AO1 (understanding)** **Asynchronous:** Receiver and transmitter are not synchronised by a common clock // receiver's clock synchronised to transmitter's each time a start bit is received // receiver and transmitter clocks synchronised for duration of a transmission; **Synchronous:** Receiver and transmitter (continuously) synchronised by a common clock // timing information transmitted within/alongside the data // receiver and transmitter clocks are (continuously) synchronised; **NE.** Receiver and transmitter are synchronised **Max 1**	**1**

Qu	Pt	Marking guidance	Total marks
2	1	**Mark is AO2 (analyse)** Bit rate is double / twice baud rate // baud rate is half bit rate; **A.** "It" is double **A.** 2:1	1

Qu	Pt	Marking guidance	Total marks
2	2	**Mark is AO1 (understanding)** They are (directly) proportional // the greater the bandwidth, the higher the bit rate; **A.** as bit rate increases so does bandwidth as BOD **NE.** bandwidth constrains bit rate	1

Qu	Pt	Marking guidance	Total marks
2	3	**All marks AO1 (understanding)** Serial sends one bit at a time / after each other whereas parallel sends multiple bits simultaneously/at same time; **R.** bytes, values, packets, data for bits Serial uses a single wire / cable / path / line whereas parallel uses several / multiple wires / cables / paths / lines; **NE.** answers that refer to multiple channels **Both sides of point must be made to award a mark.**	2

Question			Marks
3	1	**All marks AO1 (knowledge)** Multiple bits transmitted simultaneously / at same time; **NE.** data, values etc for bits Each (simultaneously transmitted) bit is sent down a different wire / cable / path / line; **A.** multiple wires / cables / paths / lines used for transmission	**2**

Question			Marks
3	2	**Mark is AO1 (understanding)** The hardware / wiring required for serial data transmission is cheaper; **NE.** cheaper without reference to hardware or wiring Serial transmission does not suffer from crosstalk // (two) bits cannot interfere with each other because they are not sent simultaneously; Serial transmission does not suffer from data skewing // bits transmitted are guaranteed to arrive in the order they were sent; **NE.** more reliable, lower probability of interference / corruption Serial transmission can be used over longer distances; **Max 1**	**1**

Question			Marks
3	3	**Mark is AO1 (understanding)** **B** Latency is the rate at which signals on a wire or line can change; **R.** if more than one lozenge shaded	**1**

Question			Marks
3	4	**Mark is AO1 (knowledge)** Start the receiver clock ticking; **A.** to wake up the receiver Synchronise the clock in the receiver to the transmitter clock // bring the clock in the receiver into phase with the clock in the transmitter; **A.** to synchronise the receiver and transmitter clocks **A.** synchronise the clocks in the devices **NE.** synchronise the (two) clocks **R.** indicates start of transmission **Max 1**	**1**

Question			Marks
3	5	**Mark is AO1 (knowledge)** Provides time for the receiver to process / transfer the received data; **NE.** indicates that the received data can be processed Allows the (next) start bit to be recognised; **R.** indicates end of transmission **R.** indicates clocks no longer need to be synchronised **Max 1**	**1**

Qu	Pt	Marking guidance	Total marks
4	1	**Mark is AO2 (analysis)** 2; **A.** Number not stated but identified that 4 and 5 are the valid patterns **I.** Incorrect patterns stated if correct answer 2 given	1

Qu	Pt	Marking guidance	Total marks
4	2	**Mark is AO1 (understanding)** Receiver and transmitter (continuously) synchronised by a common clock // timing information transmitted within/alongside the data // receiver and transmitter clocks are (continuously) synchronised; **A.** Both devices synchronised by same clock **NE.** Receiver and transmitter are synchronised **NE.** Transmission synchronised to a clock signal	1

Qu	Pt	Marking guidance	Total marks
4	3	**Mark is AO1 (understanding)** Errors that change an even number of bits (**A.** two bits) cannot be detected; **R.** multi-bit errors cannot be identified (Errors can be detected but) errors cannot be corrected; **A.** Position of errors cannot be identified **Max 1**	1

Qu	Pt	Marking guidance	Total marks
4	4	**Mark is AO1 (knowledge)** **A**; (Line A) **R.** If more than one lozenge shaded	1

Qu	Pt	Marking guidance	Total marks
5	1	**Mark is AO1 (knowledge)** Receiving and transmitting components share a common clock // are (continuously) synchronised by a common clock; **A.** receiver and transmitter **A.** "communicating components" without reference to receiver and transmitter Timing information transmitted within / alongside the data; Receiver and transmitter components clocks are (continuously) synchronised; **A.** receiver and transmitter **A.** "communicating components" without reference to receiver and transmitter **NE.** receiver and transmitter are synchronised **TO.** stated that synchronisation is only when data is transmitted **Max 1**	**1**

Qu	Pt	Marking guidance	Total marks
5	2	**All marks are AO1 (understanding)** **1 mark** for identifying a difference between communicating with peripherals and between components inside the computer: • data has to travel further to a peripheral // data travels a shorter distance between internal components • position of internal components is fixed // peripherals may be moved • more data is transmitted between internal components than to peripherals // data is transmitted more frequently between internal components than to peripherals // data must be transmitted at a higher rate between internal components than to peripherals. **1 mark** for giving a reason why internal buses are parallel: • more data / multiple bits can be transmitted simultaneously / at the same time. **A.** faster transmission **1 mark** for giving a reason why serial is used for connecting peripherals: • data skew cannot occur • crosstalk cannot occur • data transmission speed (on one wire) can be higher • cabling is cheaper • cabling allows more flexibility over positioning • cables can be longer. **Award marks for differences stated in reverse, eg serial communication has slower transmission is equivalent to parallel faster transmission, parallel cabling more expensive is equivalent to serial cabling cheaper.**	**3**